METHOD AND STRUCTURE FOR REDUCTION OF IMPEDANCE USING DECOUPLING CAPACITOR

Abstract of the Disclosure

A decoupling capacitor structure and its use in a circuit board mounting an ASIC is provided. The decoupling capacitor structure is arranged so that parasitic inductance caused by the connection to the decoupling capacitor and the decoupling capacitor itself is reduced. The circuit boards include at least two voltage planes. An ASIC having active device(s) is connected to one face of the circuit board. A decoupling capacitor structure is provided having at least two conductive plates in a dielectric material and is connected directly or indirectly to the ASIC. Vias extend from the conductive plates through the dielectric material to connect to circuit board vias on a second face of the printed circuit board or to the ASIC. The decoupling capacitor vias are parallel to each other; and each via connected to one conductive plate is located adjacent a via connected to another conductive plate to minimize voltage deviation.